DATA SHEET

74ABT16827A
74ABTH16827A

20-bit buffer/line driver, non-inverting (3-State)

Product specification
Supersedes data of 1998 Feb 27

2002 Dec 17

Philips
Semiconductors

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20-bit buffer/line driver, non-inverting (3-State)

74ABT16827A
74ABTH16827A

FEATURES

- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- 3-State output buffers
- Power-up 3-State
- 74ABTH16827A incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64 mA / –32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16827A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16827A 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables (n$\overline{OE}$1, n$\overline{OE}$2) for maximum control flexibility.

Two options are available, 74ABT16827A which does not have the bus-hold feature and 74ABTH16827A which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	C_L = 50 pF; V_{CC} = 5 V	1.7 1.4	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0 V or V_{CC}; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5 V	500	µA
I_{CCL}		Outputs LOW; V_{CC} = 5.5 V	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
56-Pin Plastic SSOP Type III	–40 °C to +85 °C	74ABT16827ADL	SOT371-1
56-Pin Plastic TSSOP Type II	–40 °C to +85 °C	74ABT16827ADGG	SOT364-1
56-Pin Plastic TSSOP Type II	–40 °C to +85 °C	74ABTH16827ADGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 – 1A9 2A0 – 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 – 1Y9 2Y0 – 2Y9	Data outputs
1, 56, 28, 29	1$\overline{OE}$0, 1$\overline{OE}$1 2$\overline{OE}$0, 2$\overline{OE}$1	Output enable inputs (active-LOW)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

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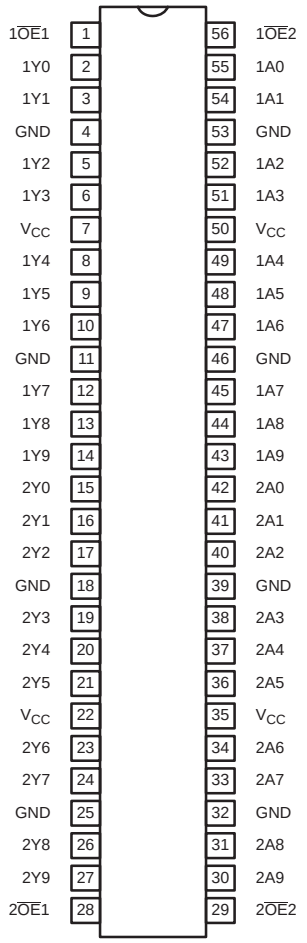
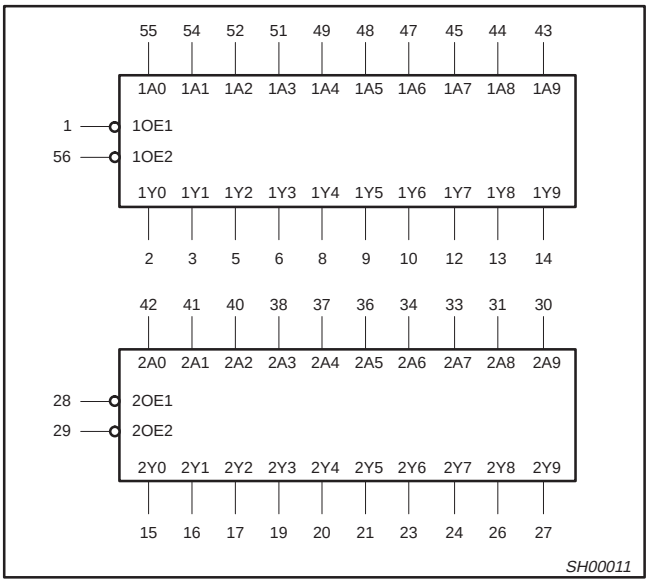
PIN CONFIGURATION



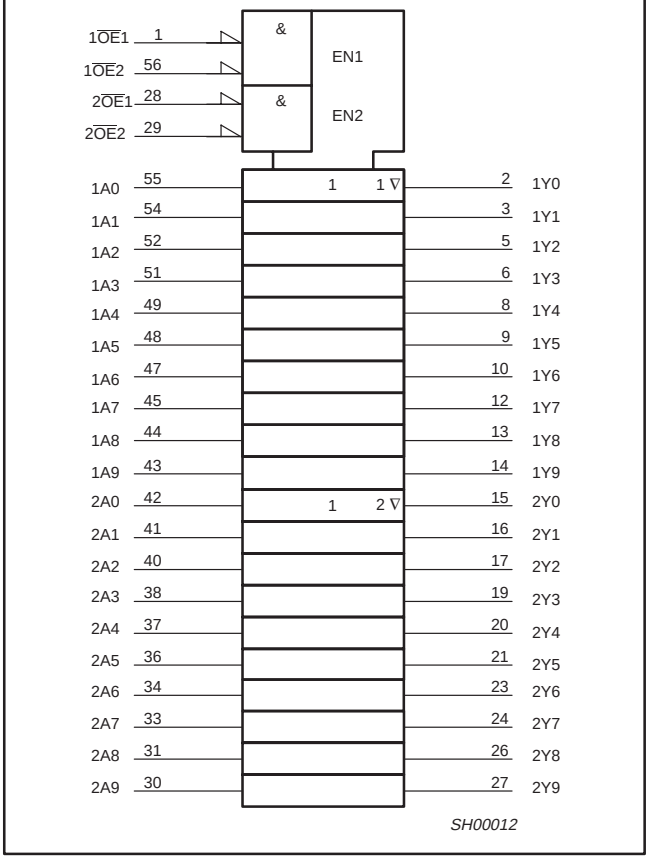
SH00010

LOGIC SYMBOL



SH00011

LOGIC SYMBOL (IEEE/IEC)



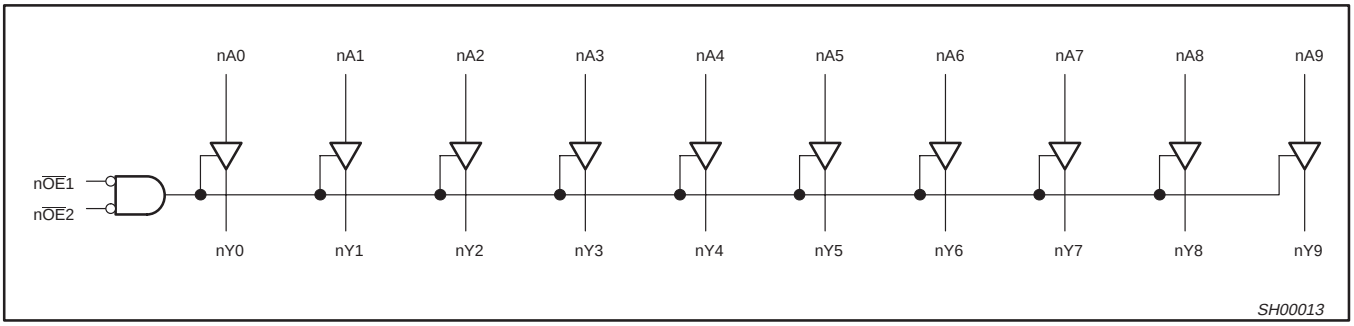
SH00012

FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
n$\overline{OE}$x	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = HIGH voltage level
L = LOW voltage level

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	–64	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	LOW-level Input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	–32	mA
I_{OL}	LOW-level output current	–	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C		
				MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA			–0.9	–1.2		–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}		2.5	2.9		2.5		V
		V_{CC} = 5.0 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}		3.0	3.4		3.0		V
		V_{CC} = 4.5 V; I_{OH} = –32 mA; V_I = V_{IL} or V_{IH}		2.0	2.4		2.0		V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}			0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V			±0.01	±1.0		±1.0	µA
I_I	Input leakage current 74ABTH16827A	V_{CC} = 5.5 V; V_I = 5.5 V			0.01	1		1	µA
		V_{CC} = 5.5 V; V_I = V_{CC} or GND	Control pins		±0.01	±1		±1	µA
		V_{CC} = 5.5 V; V_I = V_{CC}	Data pins[4]		0.01	1		1	µA
		V_{CC} = 5.5 V; V_I = 0			–1	–3		–5	µA
I_{HOLD}	Bus Hold current A inputs[5] 74ABTH16827A	V_{CC} = 4.5 V; V_I = 0.8 V		35			35		µA
		V_{CC} = 4.5 V; V_I = 2.0 V		–75			–75		
		V_{CC} = 5.5 V; V_I = 0 to 5.5 V		±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0 V; V_O = 4.5 V; V_I = 0 V or 5.5 V			±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OE} = Don't care			±5.0	±50		±50	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5 V; V_O = 2.7 V; V_I = V_{IL} or V_{IH}			1.0	10		10	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}			–1.0	–10		–10	µA
I_{CEX}	Output HIGH leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}			1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5 V; V_O = 2.5 V		–50	–70	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5 V; Outputs HIGH, V_I = GND or V_{CC}			0.5	1		1	mA
I_{CCL}		V_{CC} = 5.5 V; Outputs LOW, V_I = GND or V_{CC}			9	19		19	mA
I_{CCZ}		V_{CC} = 5.5 V; Outputs 3-State; V_I = GND or V_{CC}			0.5	1		1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND			0.2	1		1	mA

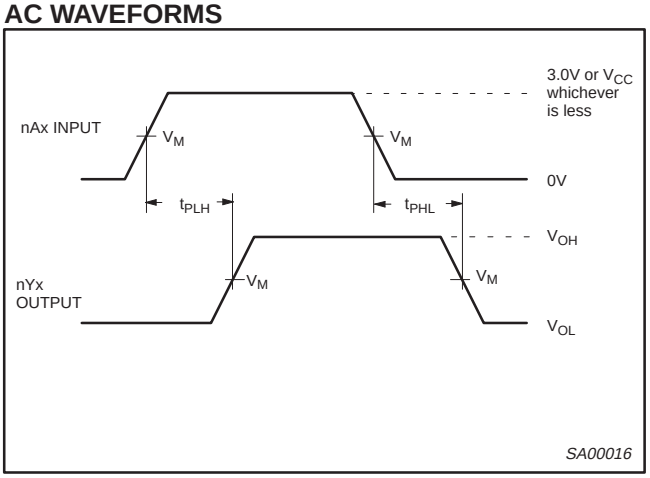
NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4 V.
3. This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10% a transition time of up to 100 µsec is permitted.
4. Unused pins at V_{CC} or GND.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

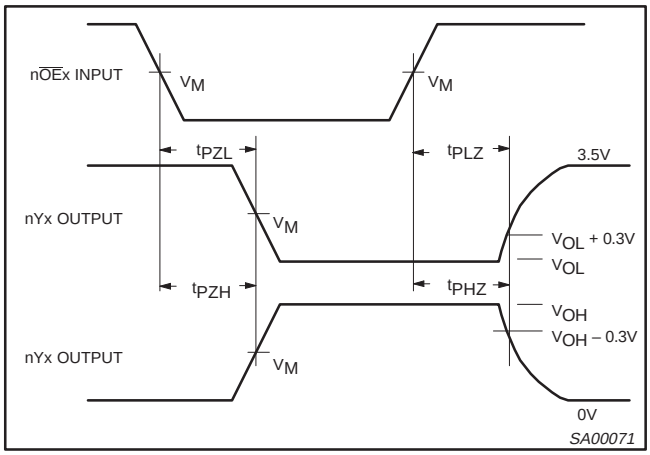
GND = 0 V, t_R = t_F = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V			T_{amb} = –40 °C to +85 °C V_{CC} = +5.0 V ±0.5 V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nYx	1	1.0 0.6	1.7 1.4	2.4 2.0	1.0 0.6	2.7 2.3	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	2	1.0 1.0	3.0 3.0	4.1 4.0	1.0 1.0	5.0 5.0	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	2	2.0 1.6	3.2 2.4	4.3 3.2	2.0 1.6	5.0 3.5	ns

AC WAVEFORMS

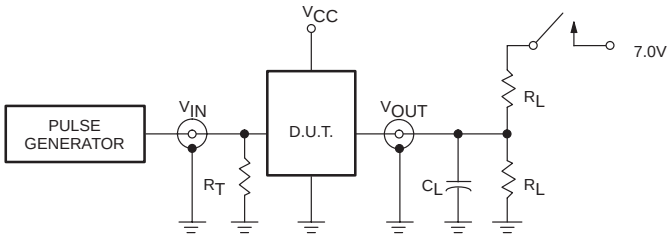


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

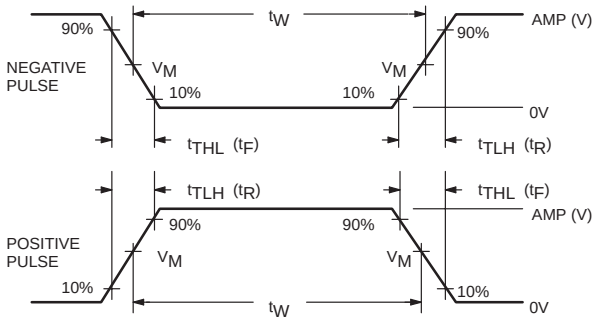


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

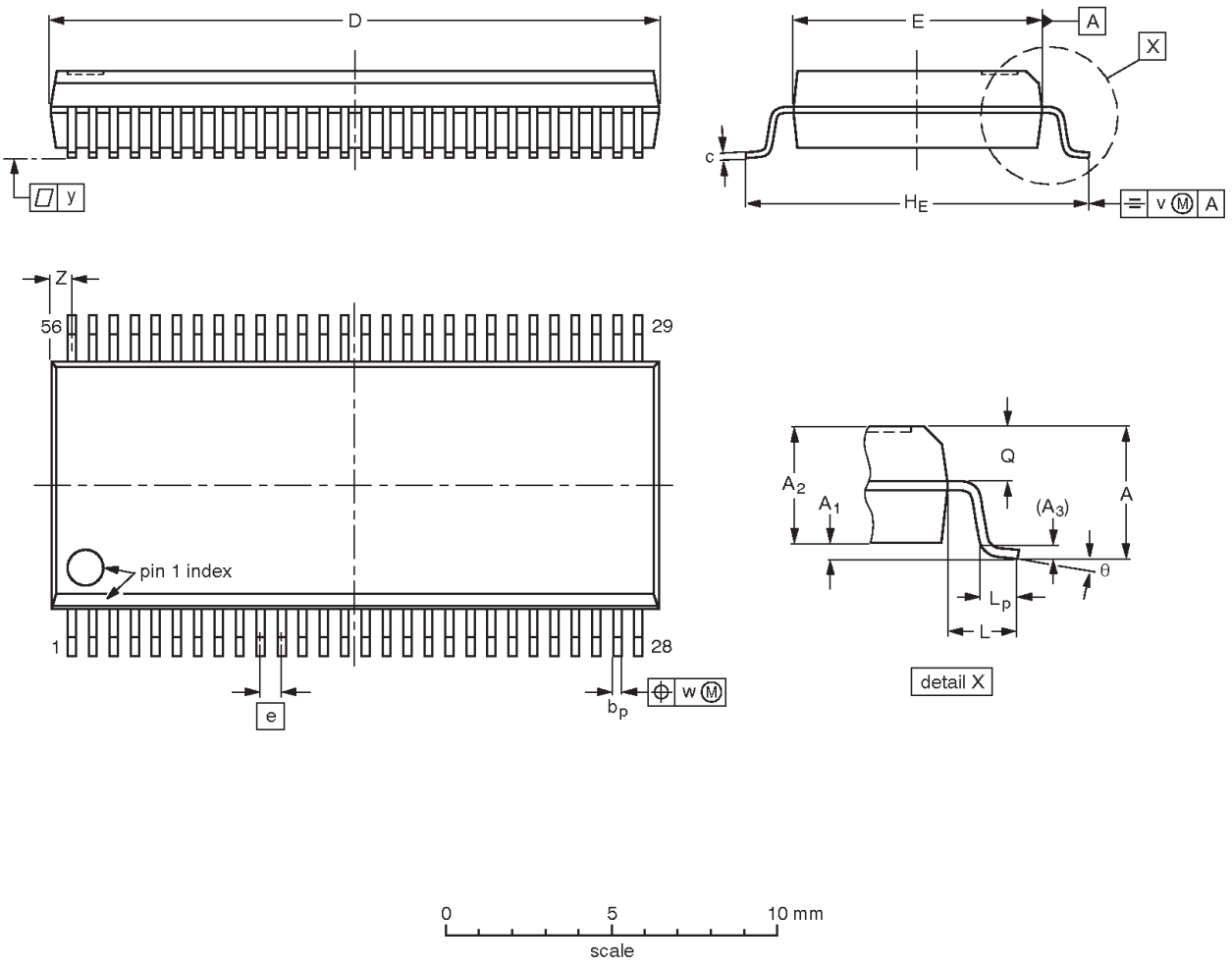
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

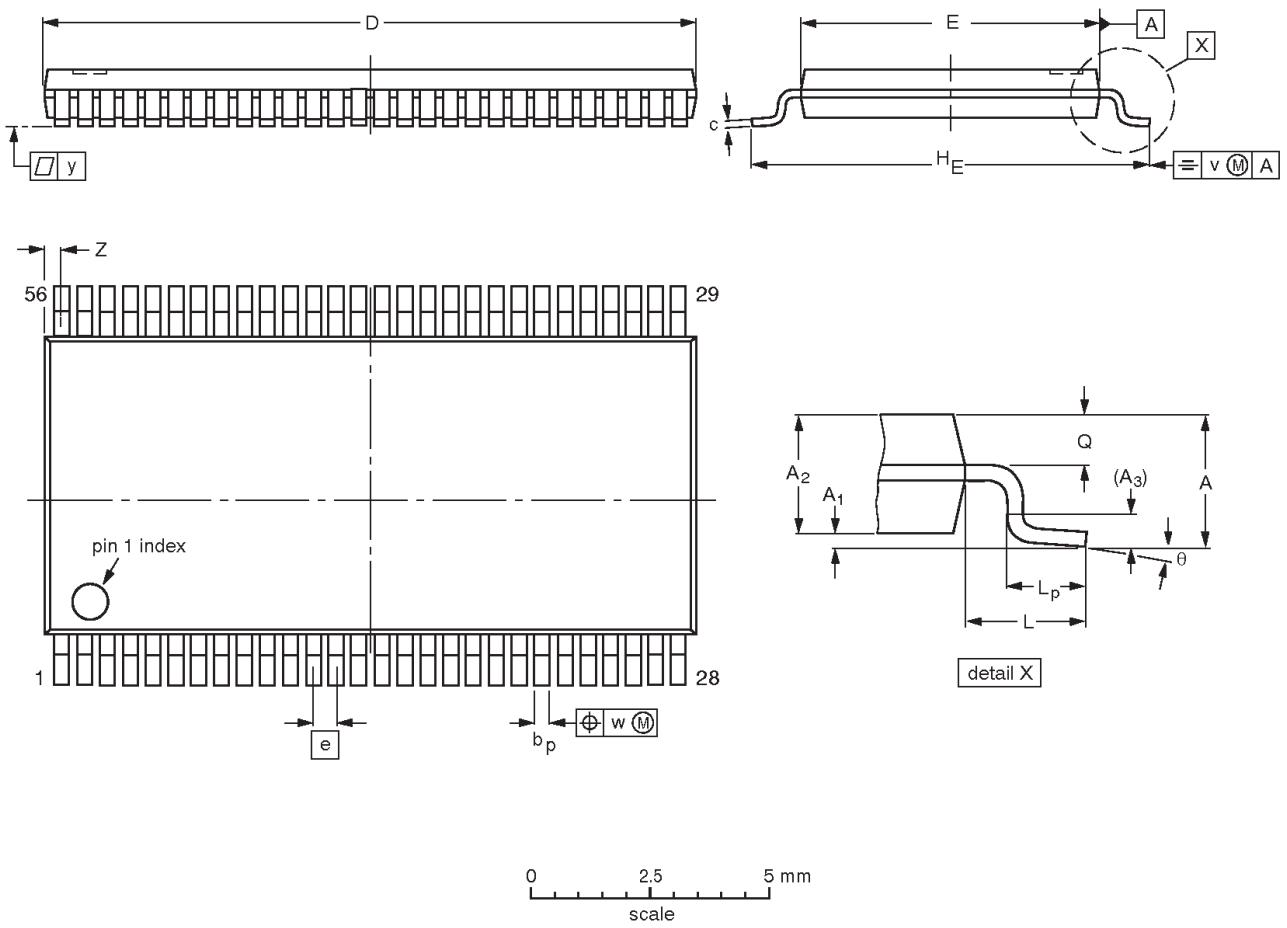
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118				~~95-02-04~~ 99-12-27

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153					~~95-02-10~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_2	20021217	**Product data (9397 750 10858); ECN 853-1824 29295 of 12 December 2002. Supersedes data of 27 February 1998 (9397 750 03504).** Modifications: ● Ordering information table: remove “North America” column; remove 74ABTH16827ADL package offering.
_1	19980227	**Product specification (9397 750 03504). ECN 853-1824 19025 of 27 February 1998.**

20-bit buffer/line driver, non-inverting (3-State)

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Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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